TECHNICAL REPORT

TR-338

Reverse Power Feed Testing

Issue: 1

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List of Figures

List of Tables

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Executive Summary

This Broadband Forum Technical Report, TR-338 serves as the test plan for the Reverse Power Feed (RPF) testing for the Power Source Equipment (PSE) implementations according to ETSI specification TS 101 548 [2]. Technical content in this test plan includes test setup information, equipment configuration requirements, test procedures and pass/fail requirements for each test case. Specifically, it includes functional and safety test cases for the PSE standalone test setup, in which a single-line Gfast DPU implementation (e.g., DPU emulator) only includes the reverse powering features specified in [2].

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1 Purpose and Scope

1.1 Purpose

With short copper loops required by G.fast Distribution Point Units (DPUs) that push the deployment of the DPUs closer to the customer premise, local power and forward power may not be available at the deployment location. To power the DPU, power will come from the customer premises location over the copper pair used for data transmission; this is referred to as Reverse Power Feed (RPF).

This document specifies a set of test cases and related pass/fail requirements for reverse powering (RPF) of remote network nodes (Gfast DPUs, single-port or multi-port) from customer premises equipment (one or multiple CPEs). Specifically, it defines functional and safety test cases for Power Source Equipment (PSE) implemented according to ETSI specification TS 101 548 [2], either as a stand-alone device or as a function integrated in a G.fast (G.9700 [3] and G.9701 [4]) Network Termination and reversely powering DPU implementations (TR-301 Issue 2 [1]). Issue 1 of TR-338 focuses on a PSE standalone tests in the test setup in which a DPU implementation only includes the reverse powering features specified in [2].

Test cases are mainly specified with reference to ETSI TS 101 548 [2] and BBF TR-301 Issue 2 [1] requirements. Furthermore they are designed to ensure safe deployment of RPF equipment.

1.2 Scope

This document applies to RPF functions of a DPU and customer premises Power Source Equipment (PSE) claiming compliance to ETSI TS 101 548 [2]. Issue 1 of this document includes test cases specific to the PSE only.

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2 References and Terminology

2.1 Conventions

In this Technical Report, several words are used to signify the requirements of the specification. These words are always capitalized. More information can be found be in RFC 2119 [7].

SHALL	This word, or the term "REQUIRED", means that the definition is an absolute requirement of the specification.
SHALL NOT	This phrase means that the definition is an absolute prohibition of the specification.
SHOULD	This word, or the term "RECOMMENDED", means that there could exist valid reasons in particular circumstances to ignore this item, but the full implications need to be understood and carefully weighed before choosing a different course.
SHOULD NOT	This phrase, or the phrase "NOT RECOMMENDED" means that there could exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications need to be understood and the case carefully weighed before implementing any behavior described with this label.
MAY	This word, or the term "OPTIONAL", means that this item is one of an allowed set of alternatives. An implementation that does not include this option MUST be prepared to inter-operate with another implementation that does include the option.

2.2 References

The following references are of relevance to this Technical Report. At the time of publication, the editions indicated were valid. All references are subject to revision; users of this Technical Report are therefore encouraged to investigate the possibility of applying the most recent edition of the references listed below.

A list of currently valid Broadband Forum Technical Reports is published at www.broadband-forum.org.

Document	Title	Source	Year
[1] TR-301 Issue 2	*Architecture and Requirements for Fiber to the Distribution Point*	BBF	2017
[2] ETSI TS 101 548-1 v2.2.1	*European Requirements for Reverse Powering of Remote Access Equipment; Part 1: Twisted pair networks*	ETSI	2018

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[3] G.9700	*Fast Access to Subscriber Terminals (G.fast) – Power spectrum density specification*	ITU-T	2014
[4] G.9701	*Fast Access to Subscriber Terminals (G.fast) – Physical layer specification*	ITU-T	2014
[5] G.997.2 Amd 4	*Physical layer management for G.fast transceivers (2016) Amendment 4*	ITU-T	2017
[6] EN 62368-1	*Audio/video, information and communication technology equipment - Part 1: Safety requirements*	CENELEC	2014
[7] RFC 2119	*Key words for use in RFCs to Indicate Requirement Levels*	IETF	1997

2.3 Definitions

The following terminology is used throughout this Technical Report.

Gfast	Marketing term for G.fast
Mains Supply	AC electricity power supply
Normal operation	State of a system (i.e., a DPU reversely powered by a PSE) reached after the start-up procedure has been completed
Start-up operation	Start-up procedure of a system (powering part of a DPU and PSE)
POTS Remote Copper Reconfiguration (RCR)	RCR refers to the Scenario where POTS from the exchange may be provided to the subscriber and shall be disconnected by the DPU, prior to start-up of the DPU. This is an optional extension of the MDSU protocol on lines where POTS may be present. Refer to clause 6.2.5.1 in [2].
One-box solution	Power Source Equipment (PSE) is integrated in the same physical entity as CPE
Two-box solution	Power Source Equipment (PSE) is a stand-alone device and not integrated in the same physical entity as CPE
PoE	Power over Ethernet describes any of several standards (IEEE 802.3) which pass electric power along with data on twisted pair Ethernet cabling
PoE PD	PoE Powered Device

2.4 Abbreviations

This Technical Report uses the following abbreviations:

AC	Alternating Current
CPE	Customer Premises Equipment
CPE ME	CPE Management Entity

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DC	Direct Current
ELC	Error Line Condition
DPU	Distribution Point Unit
DPU ME	DPU Management Entity
FTTdp	Fiber to the distribution point
FTU	G.fast Transceiver Unit
FTU-O	FTU at the Optical Network Unit (i.e., operator end of the line)
FTU-R	FTU at the Remote site (i.e., subscriber end of the line)
G.fast	Fast Access to Subscriber Terminals
MDSU	Metallic Detection Start-Up
MELT	Metallic Line Testing
NMS	Network Management System
NT	Network Termination
PRP	Protocol for RCR
PE	Power Extractor
PHY-L	Physical Layer
POTS	Plain Old Telephone Service
PS	Power Splitter
PSE	Power Source Equipment
PSU	Power Supply Unit
RCR	Remote Copper Reconfiguration
RPF	Reverse Power Feed
SUT	System Under Test
UPS	Un-interruptible Power Supply

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3 Technical Report Impact

3.1 Energy Efficiency

TR-338 has no impact on energy efficiency.

3.2 Security

TR-338 has no impact on security.

3.3 Privacy

Any issues regarding privacy are not affected by TR-338.

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4 Common Test Information

4.1 Compliance Requirements

The tests contained in this document are intended to verify that a Power Source Equipment (PSE) complies with the functional i.e., powering, electrical and safety requirements of ETSI technical specification TS 101 548 [2].

4.2 Test Plan Passing Criteria

The tests contained in this document are each marked with a test status, indicating: “mandatory”, “conditional mandatory” or “optional.”

Tests marked as “mandatory” SHALL be performed when completing testing according to this test plan.

Tests marked as “conditional mandatory” also include a conditional statement; which if met, indicates the test SHALL be considered as “mandatory.” If the conditional statement is not met, the test SHALL be considered as “not applicable.”

Tests marked as “optional” MAY be completed at the request of the tester or equipment manufacturer.

For the purpose of determining a summary result, such as indicating a device “passes TR-338 testing,” the device SHALL pass all “mandatory” tests and all applicable “conditional mandatory” tests. “Optional” tests SHALL not impact the summary result.

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5 Equipment Features

5.1 System Information

Figure 5-1 illustrates the functional reference model of the reversely powered DPU in a typical FTTdp deployment. The main functional blocks DPU, CPE and the reverse power feed system (RPF) are shown for line 1 of N lines connected to a DPU.

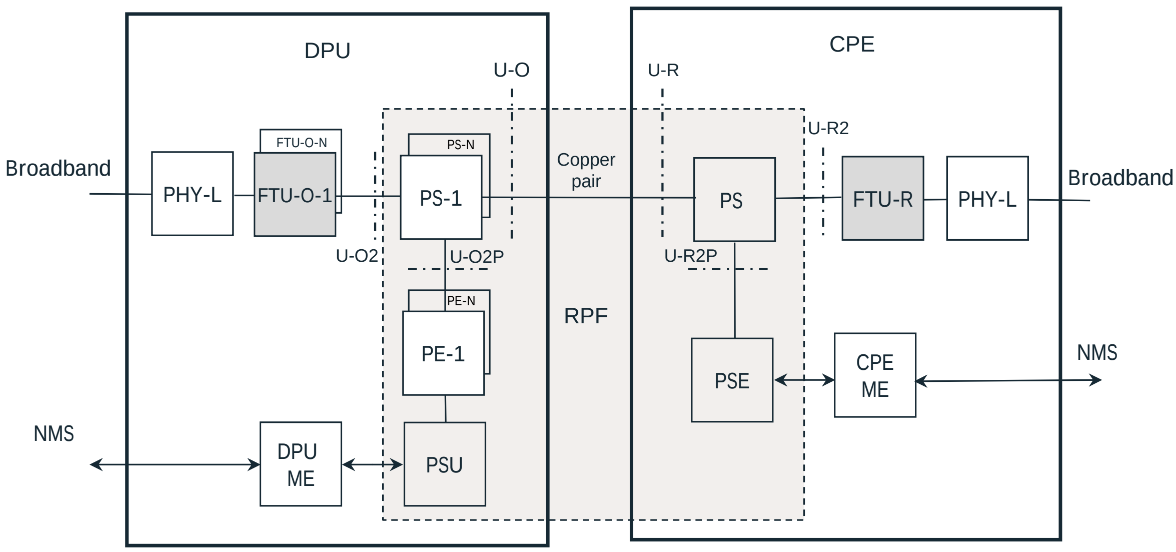

Figure 5-1 – Functional reference model of the reversely powered DPU in a typical FTTdp deployment

The FTU-O is located inside the distribution point unit (DPU) at the network side of the wire-pair (U-O reference point). The FTU-R is located at the customer premises side of the wire-pair (U-R reference point). The management of a DPU and CPE is performed by the network management system (NMS), passing management information to each management entity (DPU ME and CPE ME). The PHY-L blocks represent the physical layer of the DPU towards the access network and of the NT towards the customer premises, and the layer 2 and above functionalities contained in the DPU and the NT. The power is inserted on the line by the Power Source Equipment (PSE) located in the customer premises and extracted from the line by the Power Extractor (PE) located in the DPU. Power is extracted from each active port and combined in the Power Supply Unit (PSU). The PE and PSU are separated from the broadband signal on the line (at reference point U-O and U-R) by a power splitter (PS).

The DPU SHALL support the DPU-northbound management protocol that allows the ability to configure and retrieve the G.997.2 [5] managed objects used in this test plan. The management protocol is vendor discretionary.

The CPE is managed through the DPU-MIB and the G.9701 initialization/eoc/RMC. No LAN-side management protocol is required for the execution of this test plan, except as required to configure the CPE to pass Ethernet traffic between the G.fast and LAN interface(s).

In case of a 1-box solution where the PSE is in the same physical entity as the CPE, the RPF indications and OAM parameters shall be exchanged between the CPE ME and DPU ME using the G.997.2 RPF OAM management protocol. Otherwise, in case of a 2-box solution,

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ETSI TS 101 548 specification provides the foundation for the RPF parameters and indications that are exchanged between the PSE and the DPU.

Table 5-1, Table 5-2, and Table 5-3 are intended to provide test engineers and readers of the test report with sufficient information about the system (DPU, CPE and RPF) in order to ensure repeatability of results and to allow for accurate comparisons of reported test results. The tables SHALL be populated prior to the start of the testing and SHALL be included as part of the test report. All fields SHALL be populated; if an item is not applicable, the item MAY be marked as "Not Applicable".

Table 5-1 – DPU Information

Parameter	Reference section in G.997.2
DPU system vendor ID (DPU_SYSTEM_VENDOR)	7.13.2.1
DPU system serial number (DPU_SYSTEM_SERIALNR)	7.13.2.3
FTU O ITU-T G.994.1 vendor ID (FTUO_GHS_VENDOR)	7.13.1.1
FTU O version number (FTUO_VERSION)	7.13.1.3
Support of POTS Remote copper reconfiguration Protocol (PRP)	A.6.2.7
Maximum DPU reach resistance Rreach,dpu (7.5.2.1 of [ETSI TS 101 548])	
DPU power class (SR1, SR2 or SR3) (7.2 of [ETSI TS 101 548])	
Total number of ports (N)	

Table 5-2 – CPE Information

Parameter	Reference section in G.997.2
NT system vendor ID (NT_SYSTEM_VENDOR)	7.13.2.2
NT system serial number (NT_SYSTEM_SERIALNR)	7.13.2.4
FTU R ITU-T G.994.1 vendor ID (FTUR_GHS_VENDOR)	7.13.1.2
FTU R version number (FTUR_VERSION)	7.13.1.4

Table 5-3 - RPF Information

Parameter	Reference section in G.997.2
PSE in the same physical entity with CPE (1-box solution)	A.7.6.2.1
PSE Product Name/Model if not integrated with CPE (2-box solution)	
PSE power class (SR1, SR2 or SR3) (7.2 of [ETSI TS 101 548])	
Battery backup available at the PSE	A.7.6.2.2
Support of POTS Remote copper reconfiguration Protocol (PRP)	A.7.6.2.3
Power splitter (external) Product Name/Model	

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6 Test Environments

6.1 Test setup

This section specifies the test setups applicable to this Test Plan.

6.1.1 PSE standalone test setup

In this test plan the Gfast DPU is replaced by a DPU emulator.

The test setups below contain a number of circuits (e.g., DPU signature and power classification, etc.) and test instruments (e.g., voltage and current meter, electronic load). Details about these elements are provided in the sections below. Figures show only the case of a PSE with internal power splitter and the related interface named U-R. The voltage and current meter shown in the test setups below have time domain measurement capabilities.

Figure 6-1 shows the test configuration for PSE compliance tests to the electrical characteristics of short range power classes of ETSI TS 101 548 [2] and tests for the DPU signature detection and RPF power classification.

This configuration comprises an emulated DPU RPF front-end which includes the DPU Signature detection and RPF Power Classification circuits. These circuits are designed to operate over lower voltage ranges than nominal RPF voltage, not overlapped between each other.

The following describes the basic theory of operation of the RPF systems and is intended to aid the reader in understanding the purpose of the test setup(s). All values are provided for information purposes only, and the reader is encouraged to refer to the ETSI TS 101 548 [2] for the normative values.

The PSE performs fault detection first; if no fault is detected then it proceeds to the signature detection phase.

Then the PSE performs the DPU signature detection first (over a 2.8V-10V range) and the DPU disconnects the resistor signature if the voltage is larger than 10.1V - 12.8V.

Then the PSE performs the power classification (over a 14.5V - 20.5V range on the DPU side) and if the expected RPF Power Classification circuit (i.e., the expected I_{CLASS}) is detected the PSE increases the voltage and the power classification circuit is disconnected. Only after these two recognition phases are completed the PSE increases the voltage up to its steady-state value.

The DPU Signature circuit and the RPF Power Classification circuit are specified in sections 6.1.1.1 and 6.1.1.2 respectively. The behavior of the Electronic Load for a proper execution of the test for PSE characterization is described in section 6.1.1.3.

Figure 6-1 through Figure 6-3 below show only the PSE, regardless of this being a stand-alone device or a function integrated with a NT Module/CPE. Furthermore the powering of the PSE (i.e., mains supply or battery supply) is not shown.

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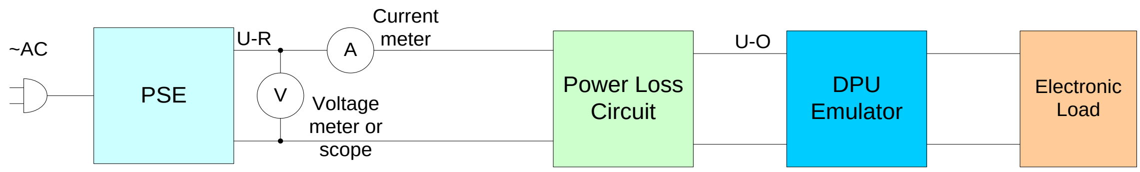

Figure 6-1- Test setup for PSE electrical compliance and DPU signature detection and power classification

Figure 6-1shows a simplified schematic of PSE test setup using an electronic load as the load termination. For electronic loads, the desired output current SHOULD be adjusted in constant current mode.

Figure 6-2 shows the test configuration for PSE tests involving fault conditions (e.g., startup with/without fault conditions, fault detection during normal PSE and DPU operation). The power class of the PSE and of the DPU (as implemented in its Power Classification circuit) shall match together [2].

The ELC (i.e., fault or Error Line Condition) insertion and Power Loss circuit are specified in sections 6.1.1.4 and 6.1.1.5 respectively.

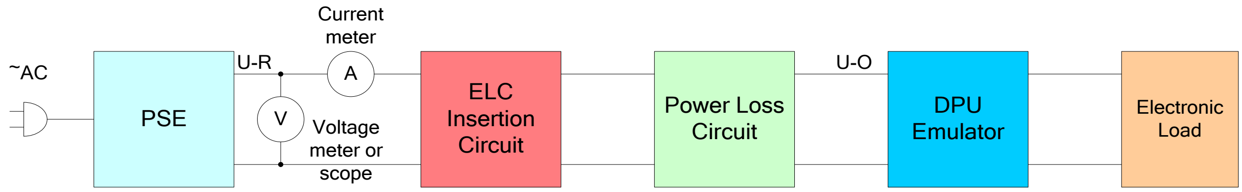

Figure 6-2 – Test setup for PSE tests in presence of faults

The setup in Figure 6-2 requires the ability to collect a time domain measurement of the voltage and current on the line. For example this could be implemented via an oscilloscope with two channels used to measure the V_{DC} (through a differential probe) and the I_{DC} (through a differential probe) with a triggered measurement start.

Figure 6-3 shows the test setup for compliance of the PSE startup in the presence of MELT signature. The MELT signature is defined in section 6.1.1.6.

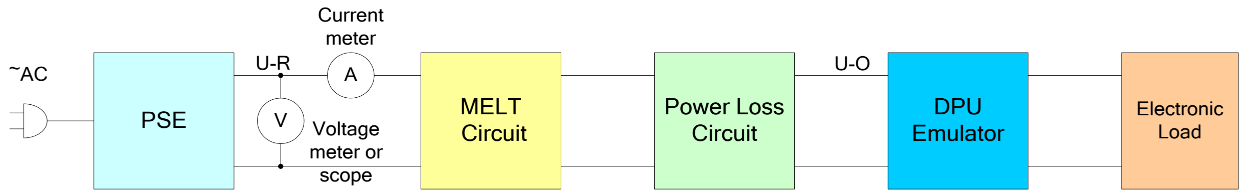

Figure 6-3 – Test setup for compliance of PSE startup in presence of MELT signature

Figure 6-4 shows the test setup for testing PSE detection of the off-hook phone during startup and normal operation.

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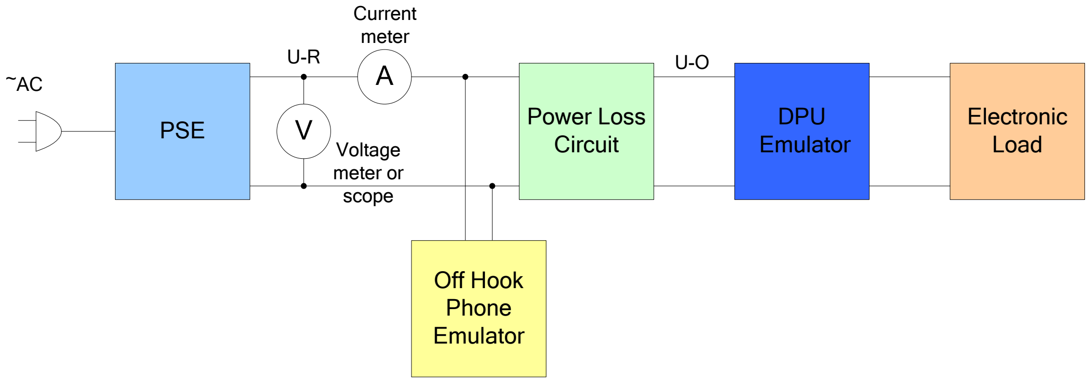

Figure 6-4 - Test setup for PSE tests in presence of off-hook phone emulator

Figure 6-5 shows the test setup for testing PSE power class with DPU power signature defined as a pulse current with amplitude 10mA, pulse duration 75ms and period 325ms.

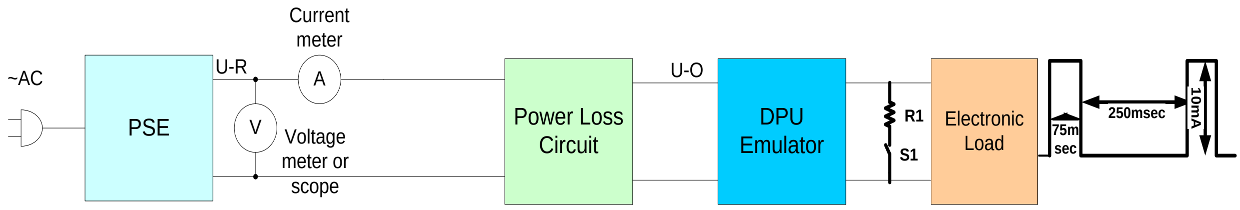

Figure 6-5 - Test setup for PSE power class with DPU power signature defined as a pulse impulse

6.1.1.1 DPU Signature circuit

The DPU Signature circuit emulates the one implemented in a DPU and it is shown in Figure 6-6. A mechanical or solid-state switch shall be located in series with the signature circuit and it has to be controlled such that the signature circuit is applied or removed during the appropriate phases of the start-up protocol. An example of a control circuit can be found in Appendix A.

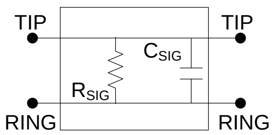

Figure 6-6 – DPU Signature circuit

The valid signature values specified in ETSI TS 101 548 [2] are reported in Table 6-1.

Table 6-1 – Valid parameter values for signature circuit

Symbol	Min	Max
$R_{V\text{-}SIG}$	23.7 kΩ	25.5 kΩ
$C_{V\text{-}SIG}$	50 nF	120 nF

ETSI TS 101 548 [2] specifies also non-valid signature values. These are reported in Table 6-2.

Table 6-2 – Non-valid parameter values for signature circuit

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Symbol	Low	High
$R_{NV\text{-}SIG}$	15 kΩ	33 kΩ
$C_{NV\text{-}SIG}$	10 µF	---

6.1.1.2 RPF Power Classification circuit

In addition to the detection signature, the DPU includes a power classification signature. The key objectives for the classification circuitry are the following:

- Establish mutual identification of PSE and DPU as enhanced validation mechanism on top of the detection mechanism. This addresses the scenario in which a combination of connected equipment (e.g., phones, fax machines, etc.) would have the same signature as those of a valid DPU.
- Provide power levels interoperability criteria between PSE power classes and DPU power consumption

During the power classification phase, the DPU SHALL present only one power classification signature (V_{CLASS}, I_{CLASS}) according to Table 6-3. A mechanical or solid-state switch shall be located in series with the classification signature and it has to be controlled such that the classification signature is applied or removed during the appropriate phases of the start-up protocol. An example of a control circuit can be found in Appendix I.

Table 6-3 – Power Classification signature

Power classification signature	Voltage V_{CLASS} at DPU	Current I_{CLASS} (min)	Current I_{CLASS} (max)
Class SR1	14.5V to 20.5V	9 mA	12 mA
Class SR2		17 mA	20 mA
Class SR3		26 mA	30 mA

During the power classification phase, the PSE SHALL apply the voltage (V_{CLASS_PSE}) between 16.5V and 20.5V (section 6.2.2 in [2]) and detect the RPF Power Class based on the measured current (I_{CLASS_MEAS}) according to Table 6-4.

Table 6-4 – RPF Power Class detection

RPF power class	Voltage V_{CLASS_PSE} at PSE	Current I_{CLASS_MEAS} (min)	Current I_{CLASS_MEAS} (max)
RPF SR1	16.5V to 20.5V	8 mA	13 mA
RPF SR2		16 mA	21 mA
RPF SR3		25 mA	31 mA

6.1.1.3 Electronic Load

The Electronic Load circuit should apply the load according to Figure 6-7 :

- In 3% increments of I_{SRimax}, from 10mA to 0.95% × I_{SRimin}

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- ΔI = 5mA for SR1
- ΔI = 7.5mA for SR2
- ΔI = 10.5mA for SR3

- In 2mA increments from $0.95 \times I_{SRimin}$ to $1.05 \times I_{SRimax}$
- Step time $T_{STEP} = \geq 30$ms

Note: If measurements are performed manually, T_{STEP} could be increased to allow manual measurements of voltage, current, and power.

- Rise time T_{RISE} = 20ms

Note: The rate of change of current shall not exceed 1mA/µs (Table 37 in [2]).

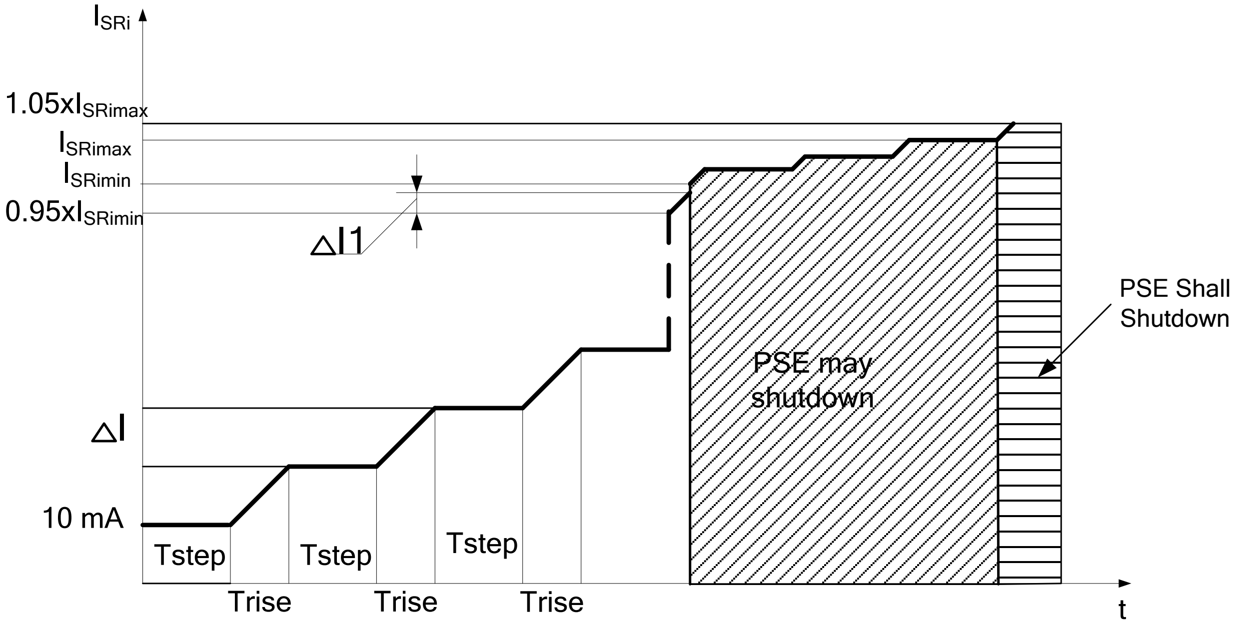

Figure 6-7 – Electronic Load (I_{SRi}) increments

6.1.1.4 Error Line Condition (ELC) circuit

The equivalent network model of the above Error Line Condition (ELC) circuit shown in Figure 6-8 is defined in section 6.1.1 in [2]. In practical implementations all ELC functions (Fig 6-7, Fig 6-2, Fig 6-4) MAY be combined into a single test setup.

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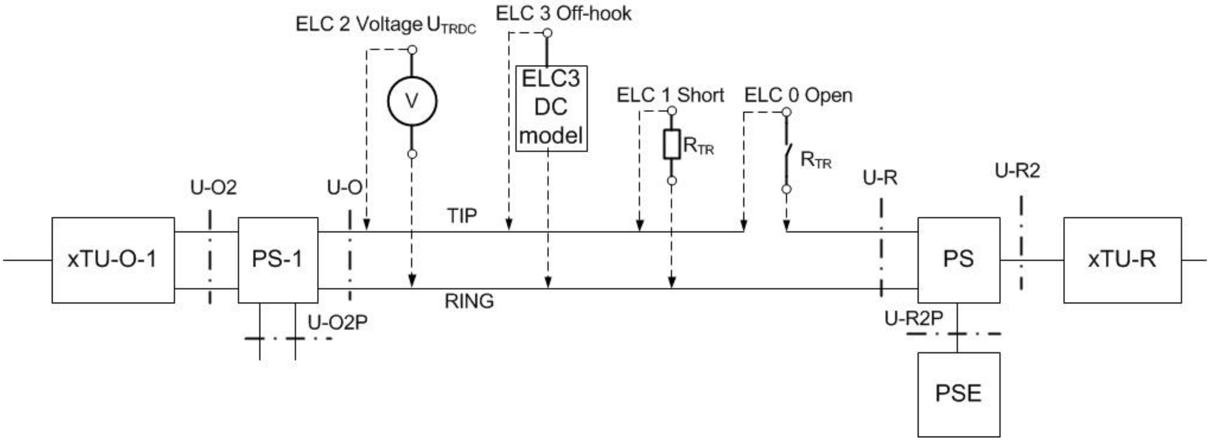

Figure 6-8 – ELC reference diagram

The Error Line Condition parameters and detection criteria for the ELC network model are defined in Table 6-5.

Table 6-5 – Error Line Condition Parameters and Detection Criteria

Error Line Condition	Description	Parameter	Detection Criteria
ELC0	Open tip-to-ring	R_{Emin} = 1 MΩ C_{Emax} = 100 nF	$R_{TR} \geq R_{Emin}$ for a duration exceeding 300ms (see NOTE 1) $C_{TR} \leq C_{Emax}$
ELC1	Short tip-to-ring	R_{Emax} = 140 Ω	$R_{TR} \leq R_{Emax}$
ELC2	POTS Exchange (foreign) DC voltage	$U_{TRDCEmax}$= 3 V	$\lvert U_{TRDC}\rvert \geq U_{TRDCEmax}$
ELC3	Off-hook phone	Measured voltage and current in the range below the upper limit of the DC characteristics defined in Table 6-6.	

NOTE 1: This duration is set such that the definition of ELC0 does not overlap with the Maintain Power Signature definition as defined in Note 4 of Table 39 in [2].

NOTE 2: Due to the definition of parameters, definite detection of ELC1 or ELC3 may be ambiguous.

Feed resistance of ELC2 voltage source SHALL be 500Ω.

The off-hook phone emulator circuit of Figure 6-9 may be used to implement the ELC3 condition.

The upper limits of the off-hook phone DC characteristics in Table 6-6 are specified in Table 9 in [2].

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Table 6-6 - Upper limits of the Off-hook phone DC voltage/current characteristics

Point	Voltage (V)	Current (mA)
A	9	0
B	9	20
C	14.5	42
D	40	50
E	60	56
NOTE: Linear interpolation of voltage in function of current shall be used to obtain values between points A-E.		

6.1.1.5 Power Loss Circuit

This section specifies the Power Loss circuit used to model a loop resistance R_{loop}, which is defined as the total DC resistance measured between the two conductors at one reference point while shorting the other two conductors at the other reference point:

- Loop resistance between U-O and U-RP2 is illustrated in Figure 29 [2]
- Loop resistance between U-O and U-R is illustrated in Figure 30 [2]

Loop resistance shall be implemented via a resistive network with fixed or tunable resistances at DC expressed in Ωs. This resistive value includes the copper loop resistance and any additional resistance between the above interfaces (e.g., a connector, over-current protectors, a power splitter). The resistive circuit is shown in Figure 6-9.

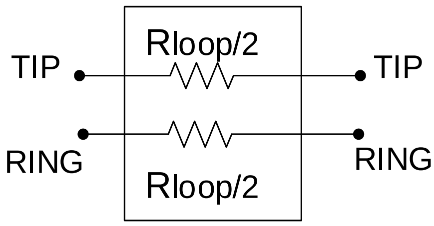

Figure 6-9 – Resistive network for power loss circuit

The R_{loop} values for the power loss circuit of are listed in Table 6-7. These values roughly represent 20, 50, 100, 200, and 250 m loop lengths of cable with a loop resistance of 0.168Ω/m (0.5 mm section).

Table 6-7 – R_{loop} values for power loss circuit

	Nominal value
R1	4Ω ± 5 %
R2	8Ω ± 5 %
R3	16Ω ± 5 %
R4	34Ω ± 5 %
R5	43Ω ± 5 %

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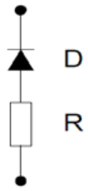
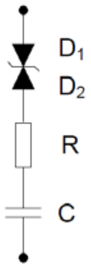
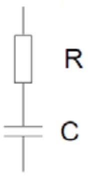
6.1.1.6 MELT signature

MELT signatures located at the U-R interface are defined in section 6.1.2 in [2].

Table 6-8 – MELT signatures

<table>
<tr><th></th><th></th><th>MELT signature</th><th>Comments</th></tr>
<tr><td>1</td><td>
</td><td><table><tr><td>Component</td><td>Nominal value</td></tr><tr><td>R</td><td>470kΩ+/-1%</td></tr><tr><td>$U_{F(D)}$</td><td>0.7V (at I_f=10mA) +/- 0.1V</td></tr></table></td><td>DR type
Specified in TR-286</td></tr>
<tr><td>2</td><td>
</td><td><table><tr><td>Component</td><td>Nominal value</td></tr><tr><td>R</td><td>100kΩ +/- 1%</td></tr><tr><td>C</td><td>470nF +/- 1%</td></tr><tr><td>$U_{Z(D1)}$</td><td>6.8V +/- 5% @ 50µA</td></tr><tr><td>$U_{Z(D2)}$</td><td>6.8V +/- 5% @ 50µA</td></tr></table></td><td>ZRC type
Specified in TR-286</td></tr>
<tr><td>3</td><td>
</td><td><table><tr><td>Component</td><td>Nominal value</td></tr><tr><td>R</td><td>20kΩ +/- 1%</td></tr><tr><td>C</td><td>2.2µF +/- 10%</td></tr></table>NOTE 1: time constant t = R×C ≤ 49ms.
NOTE 2: additional constraint for PSE supporting POTS Remote copper reconfiguration Protocol (PRP) is a resistive part exceeding 4kΩ.</td><td>RC type</td></tr>
</table>

6.1.1.7 Off-hook phone emulator circuitry

This section specifies an off-hook phone emulator circuit which shall be used for testing the PSE detection of the off-hook phone. The purpose of this circuit is to emulate off-hook phone detection on a PSE startup and powering mode and meet requirements for off-hook phone specification according to ETSI TS101 548 Table 9, and take into account Table 37 (Note 5).

The off-hook emulator circuitry is presented in Figure 6-10.

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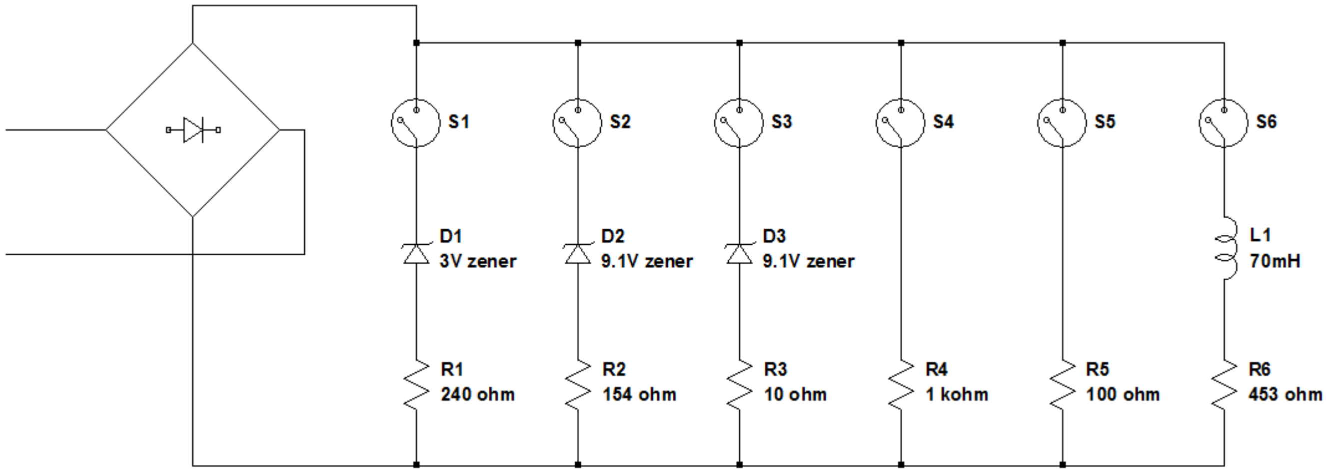

Figure 6-10 - Off-hook emulator circuitry

Purpose of switches S1 to S5 is to emulate the off-hook phone behavior during different phases of RPF PSE operations: detection, classification and normal operation when PSE is powering DPU according to the voltage/current characteristics of the off-hook phone defined in Table 6-6.

Off-hook phone behavior during the detection phase of PSE start up at $I_{S1@9V}$=19mA and $I_{S4@9V}$=7.6 mA is emulated with switches S1 and S4 turned on.

Off-hook phone behavior during the classification phase of PSE start up at $I_{S2@18V}$=48.7mA and $I_{S3@18V}$=750 mA is emulated with switches S2 and S3 turned on.

Off-hook phone behavior during the normal PSE operation supplying power to DPU at $I_{S4@57V}$=55.6mA and $I_{S5@18V}$=5.56A is emulated with switches S4 and S5 turned on.

Purpose of switch S6 is to test immunity of the PSE off-hook detection circuitry to load transients below 1mA/µs (Table 37 in [2]).

The off-hook emulator components are listed in Table 6-9.

Table 6-9 – Off-hook emulator components

Component	Nominal value
BR	80V-100V, 5A bridge rectifier
D1	3V+/-5% Zener diode
D2, D3	9.1V+/-5% Zener diode
R1	240Ω ± 1 %
R2	154Ω ± 1 %
R3	10Ω ± 1 %
R4	1000Ω ± 1 %
R5	100Ω ± 1 %
R6	453Ω ± 5 % (Note 1)
L1	70mH ± 10 % (Note 2, Note 3)
S1,S2,S3,S4,S5,S6	Toggle switches (Note 4)
Note 1: Resistance value of R6 includes the DC	

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resistance of inductor L1. Note 2: Parasitic capacitance of inductor L1 shall be less than 10pF. Note 3: Inductor L1 can be replaced by another electronic circuit to limit the dI/dt. Note 4: Upon closure, the toggle switch shall not limit the dI/dt below 10mA/µs.

6.1.2 DPU standalone test setup

For further study.

6.1.3 PSE and DPU system level test setup

For further study.

6.1.4 Test Setup characteristics

6.1.4.1 Temperature and humidity

The ranges of temperature and humidity of the test facility, over the entire time for which the tests are conducted, SHALL be recorded in a manner similar to that shown in Table 6-10 and SHALL be included as part of the test report.

The measured temperatures and humidities SHOULD be within the acceptable ranges below:

- temperature: between 15°C (59°F) and 35°C (95°F)
- humidity: between 5% and 85%

Table 6-10 – Temperature and Humidity Range of Test Facility

Parameter	High	Low
Temperature		
Humidity		

6.1.4.2 AC voltage

The AC voltage used to power the PSEs SHALL be recorded as shown in Table 6-11 and included in the test report.

Voltage measurements SHALL be performed three times over the entire time tests are conducted; and, in case of testing of a multi-line DPU, the voltage measurements SHALL be taken over three of the power sources to which the PSEs are connected.

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Table 6-11 – AC voltage measurements of Test Facility

Parameter	Begin test session	Middle test session	End test session
AC voltage-1			
AC voltage-2 (NOTE)			
AC voltage-3 (NOTE)			
NOTE: This applies only to multi-line DPU testing.			

The measured AC voltages SHOULD be within the acceptable ranges below depending on the region the PSE is tested for:

- Europe: 230Vac ± 10% @50Hz
- North America: 120Vac ± 10% @60Hz
- China: 220Vac ± 10% @50Hz
- Japan: 100Vac ± 10% @50Hz or 60Hz

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7 PSE standalone functional testing

Purpose of this testing is to verify that a Power Source Equipment (PSE) implementation complies with the ETSI TS 101 548 [2] requirements. Section 7 specifies functional and safety test cases for the PSE standalone test setup.

Test cases include test procedures and pass/fail requirements for different stages of PSE operation: in presence of error line conditions, during start-up and in normal operation (i.e., steady state when PSE reversely powers a DPU). These tests are applicable to the one-box and two-box solutions.

An example of a DPU emulator is given in Appendix I.

7.1 ELC testing during start-up

The purpose of this test is to verify that a PSE performs detection and protection functions during start up in presence of the following error line conditions (ELC):

- ELC0 – open circuit between tip and ring
- ELC1 – short circuit between tip and ring
- ELC2 – foreign voltage
- ELC3 – off-hook phone model

7.1.1 ELC0- open tip-to-ring test

Test requirement: Mandatory.

7.1.1.1 Test Setup

1. The PSE and the DPU emulator SHALL be connected to the test setup shown in Figure 6-2.
2. The ELC insertion circuit SHALL be set to ELC0, see Figure 6-8 and Table 6-5.
3. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
4. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
5. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
6. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.1.1.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. Disconnect the PSE from the test setup.
4. Create the ELC0 condition.
5. Reconnect the PSE to the test setup.
6. Wait 5 seconds, then measure the output voltage over a 5 second period at the PSE. Record the peak value during this period.
7. Record if the device indicated an ELC0 failure condition.
8. Remove the ELC0 condition.
9. Wait 5 seconds, then measure output voltage at the PSE.

7.1.1.3 Report

1. The measured output voltage in step 2.

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2. The measured output voltage in step 6.
3. The measured peak output voltage during step 6.
4. Report whether PSE provided indication of detected ELC0 condition [yes/no].
5. The measured output voltage in step 9.

7.1.1.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 6, the measured peak voltage on the line SHALL NOT exceed 30V.
3. In step 9, the measured output voltage SHALL be in the range of 55.75-60V.

7.1.2 ELC1-Short tip-to-ring test

Test requirement: Mandatory.

7.1.2.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-2.
2. The ELC insertion circuit SHALL be set to ELC1, see Figure 6-8 and Table 6-5.
3. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
4. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
5. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
6. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.1.2.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. Disconnect the PSE from the test setup.
4. Create the ELC1 condition.
5. Reconnect the PSE to the test setup.
6. Wait 5 seconds, then measure output voltage and current at the PSE.
7. Record if the device indicated an ELC1 failure condition
8. Remove the ELC1 condition.
9. Wait 5 seconds, then measure output voltage at the PSE.

7.1.2.3 Report

1. The measured output voltage in step 2.
2. The measured output voltage in step 6.
3. Report whether PSE provided indication of detected ELC1 condition [yes/no].
4. The measured output voltage in step 9.

7.1.2.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 6, the measured output voltage SHALL be less than 1V and the measured output current SHALL be less than 10 mA.
3. In step 9, the measured output voltage SHALL be in the range of 55.75-60V.

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7.1.3 ELC2-Foreign voltage test

Test requirement: Mandatory.

7.1.3.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-2.
2. The ELC insertion circuit SHALL be set to ELC2, see Figure 6-8 and Table 6-5.
3. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
4. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
5. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
6. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.1.3.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait for 5 seconds, then measure output voltage at the PSE.
3. Disconnect the PSE from the test setup.
4. Create the ELC2 condition by inserting the voltage of 3Vdc with Plus connected to the Tip and Minus connected to the Ring.
5. Reconnect the PSE to the test setup.
6. Wait for 5 seconds, then measure output voltage at the PSE.
7. Record if the device indicated an ELC2 failure condition.
8. Remove the ELC2 condition.
9. Wait for 5 seconds, then measure output voltage at the PSE.
10. Disconnect the PSE from the test setup.
11. Repeat steps 4-9 with the ELC2 voltage of 40Vdc and 60Vdc.
12. Reverse the polarity of the ELC2 voltage.
13. Repeat steps 5-10.

7.1.3.3 Report

1. The measured output voltage in step 2.
2. The measured output voltage in step 6.
3. Report whether PSE provided indication of detected ELC2 condition [yes/no].
4. The measured output voltage in step 9.

7.1.3.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 6, the measured output voltage SHALL NOT exceed ELC2 voltage.
3. In step 9, the measured output voltage SHALL be in the range of 55.75-60V.

7.1.4 ELC3-Off-hook phone test

This test covers the off-hook detection during the start-up phase (MDSU detection and classification).

Test requirement: Mandatory.

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7.1.4.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-4.
2. Off-hook emulator circuitry SHALL be connected with toggle switches S1…S6 in an off position (see Figure 6-10).
3. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
4. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
5. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
6. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.1.4.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. Disconnect the PSE from the test setup.
4. Turn on switch S1.
5. Reconnect the PSE to the test setup.
6. Wait 1 second, then measure output voltage at the PSE (see Note 1).
7. Turn off switch S1.
8. Wait 5 seconds, then measure output voltage at the PSE.
9. Disconnect the PSE from the test setup.
10. Turn on switch S4.
11. Reconnect the PSE to the test setup.
12. Wait 1 second, then measure output voltage at the PSE (see Note 1).
13. Turn off switch S4.
14. Wait 5 seconds, then measure output voltage at the PSE.
15. Disconnect the PSE from the test setup.
16. Turn on switch S2.
17. Reconnect the PSE to the test setup.
18. Wait 1 second, then measure output voltage at the PSE (see Note 1).
19. Turn off switch S2.
20. Wait 5 seconds, then measure output voltage at the PSE.
21. Disconnect the PSE from the test setup.
22. Turn on switch S3.
23. Reconnect the PSE to the test setup.
24. Wait 1 second, then measure output voltage at the PSE (see Note 1).
25. Turn off switch S3.
26. Wait 5 seconds, then measure output voltage at the PSE.

Note 1: Voltage measurements SHALL NOT be made during the PSE detection or classification phase, where, the PSE may injector voltage onto the line for the purpose of DPU detection or classification.

7.1.4.3 Report

1. The measured DC output voltage in steps 2, 6, 8, 12, 14, 18, 20, 24, 26.
2. Report whether PSE provided indication of detected ELC3 condition [yes/no].

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7.1.4.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 6, the measured output voltage SHALL be less than 1V.
3. In step 8, the measured output voltage SHALL be in the range of 55.75-60V.
4. In step 12, the measured output voltage SHALL be less than 1V.
5. In step 14, the measured output voltage SHALL be in the range of 55.75-60V.
6. In step 18, the measured output voltage SHALL be less than 1V.
7. In step 20, the measured output voltage SHALL be in the range of 55.75-60V.
8. In step 24, the measured output voltage SHALL be less than 1V.
9. In step 26, the measured output voltage SHALL be in the range of 55.75-60V.

7.2 Start-up tests

7.2.1 Line detection test during start-up

Purpose of this test is to ensure that a PSE can start up upon detection of the valid DPU signature. Also, to test a PSE ability to detect non-valid DPU signature values.

Test requirement: Mandatory.

7.2.1.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-1.
2. The loop resistor R_{loop} SHALL be set to 4Ω +/-5%, see Table 6-7.
3. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
4. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
5. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.2.1.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure PSE output voltage.
3. Disconnect the PSE from the test setup.
4. Set DPU signature $R_{V\text{-}SIG}$ to 33.6 K +/-1%.
5. Reconnect the PSE to the test setup.
6. Wait 5 seconds, then measure PSE output voltage over a 5 second period. Record the peak value during this period.
7. Disconnect the PSE from the test setup.
8. Set DPU signature $R_{V\text{-}SIG}$ to 14.7 K +/-1%.
9. Repeat steps 5-7.
10. Set the loop resistor R_{loop} to 43Ω +/-5%, see Table 6-7.
11. Repeat steps 1-9.

7.2.1.3 Report

1. The measured output voltage in step 2.
2. The measured peak output voltage in step 6.

7.2.1.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.

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2. In step 6, the measured peak output voltage SHALL be less than 10V.

7.2.2 Test of PSE RPF power classes and classification signature

Test requirement: Mandatory.

7.2.2.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-1.
2. The loop resistor R_{loop} SHALL be set to 4Ω +/-5%, see Table 6-7.
3. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
4. The DPU emulator Power Class resistor SHALL be set
    a. (Case 1: PSE and DPU power classes match) to the power class that corresponds to the tested PSE power class, see Table 6-4.
    b. (Case 2: PSE and DPU power classes mismatch) as follows:
        i. For PSE class SR3, set DPU emulator to class SR2 (see Table 6-4)
        ii. For PSE class SR2, set DPU class SR3 (see table 6.4)
        iii. For PSE class SR1, set DPU emulator to SR2 (see Table 6-4)
    c. (Case 3: PSE and DPU power classes mismatch) as follows:
        i. For PSE class SR3, set DPU emulator to class SR1 (see Table 6-4)
        ii. For PSE class SR2, set DPU class SR1 (see Table 6-4)
        iii. For PSE class SR1, set DPU emulator to SR3 (see Table 6-4)
5. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.2.2.2 Method of Procedure

1. Set the DPU emulator power class resistor according to Case 1 settings.
2. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
3. Wait 5 seconds, then measure output voltage at the PSE.
4. Disconnect the PSE from the test setup.
5. Repeat steps 2-4 for Case 2 and Case 3 power class settings.

7.2.2.3 Report

1. The measured output voltage in step 3.

7.2.2.4 Expected Results

1. In step 3,
    a. for Case 1: DC output voltage SHALL in the range 55.75-60V, which indicates that PSE and DPU power classes match.
    b. For Case 2: PSE voltage pulses SHALL be less than 20.5V on U-R interface, which indicates that PSE and DPU power classes do not match.
    c. For Case 3: PSE voltage pulses SHALL be less than 20.5V on U-R interface, which indicates that PSE and DPU power classes do not match.

7.2.3 Start-up in presence of MELT signature

Test requirement: Mandatory.

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7.2.3.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-3.
2. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
3. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
4. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
5. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.
6. The MELT signature SHALL be set to DR type, see Table 6-8.

7.2.3.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. Disconnect the PSE from the test setup.
4. Repeat steps 1-3 with the MELT signature set to ZRC type and RC type.

7.2.3.3 Report

1. The measured output voltage in step 2.

7.2.3.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.

7.3 Normal operation tests

The purpose of this test is to verify that the output voltage, continuous output current and continuous output power of a PSE in a normal operation state (i.e., steady state when PSE reversely powers a DPU) comply with Table 7-1. Electrical parameters in Table 7-1 are originally defined in Table 35 in [2].

PSE electrical specification applies to U-R interface when a power splitter is integrated in a PSE. When an external power splitter is used as a standalone device, Table 7-1 applies to U-R2P interface.

Table 7-1 – PSE electrical specification on U-R interface

Parameter	Symbol	Unit	Min	Max	Comments
Output voltage	V_{PSE}	V	55.75	60	Typical 57V. Total output voltage deviation, including initial set up, load/ line, temperature regulations is +5% , -2.2%. Up to 60V allow for transient conditions (NOTE 2).
Continuous output current for RPF Class SR1	I_{SR1}	mA	161	$P_{out\_SR1\text{-}MAX}/ V_{PSE}$	NOTE 1
Continuous output current for RPF Class SR2	I_{SR2}	mA	241	$P_{out\_SR2\text{-}MAX}/ V_{PSE}$	NOTE 1
Continuous output current for RPF Class SR3	I_{SR3}	mA	336	$P_{out\_SR3\text{-}MAX}/ V_{PSE}$	NOTE 1

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Continuous output power for Class SR1	P_{SR1}	W	8.98	10	$P_{SRimin}=V_{PSEmin}\times I_{SRimin}$ $P_{SRimax}=V_{PSEmax}\times I_{SRimax}$ where i is 1,2 and 3
Continuous Output power for Class SR2	P_{SR2}	W	13.44	15	
Continuous Output power Class SR3	P_{SR3}	W	18.73	21	
Overload time limit	T_{CUT}	ms	50	75	NOTE 1
Inrush current	I_{INRUSH}	mA		450	To allow startup transients, measurement should be taken during power up and 1ms after V_{PSE} > 30V.

NOTE 1:

a) The PSE shall remain in a normal operation state if I_{SRi} remains below I_{SRimin}, in absence of any fault condition.
b) The PSE shall remain in a normal operation state, in absence of any fault condition (for example ELC1) if I_{SRi} exceeds I_{SRimin} or I_{SRimax}, but for no longer than T_{CUTmin}.
c) If I_{SRi} exceeds I_{SRimin} for longer than T_{CUTmin}, the PSE may return to quiescent state; or it may remain in a normal operation state in absence of any fault condition.
d) If I_{SRi} exceeds I_{SRimax} for longer than T_{CUTmax}, the PSE shall return to quiescent state.

NOTE 2: Vpse is a PSE output voltage and is measured according to paragraph 6.2.2 of CENELEC EN 62368-1 [6].

7.3.1 PSE operation in presence of ELC1 (short tip-to-ring)

Test requirement: Mandatory.

7.3.1.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-2.
2. The ELC insertion circuit SHALL be set to ELC1, see Figure 6-8 and Table 6-5.
3. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
4. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ Ω +/-1%.
5. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
6. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.3.1.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. Create the ELC1 condition.
4. Wait 5 seconds, then measure output voltage and current at the PSE.
5. Remove the ELC1 condition.
6. Wait 5 seconds, then measure output voltage at the PSE.

7.3.1.3 Report

1. The measured output voltage in step 2.
2. The measured output voltage in step 4.
3. Report whether PSE provided indication of detected ELC1 condition [yes/no].
4. The measured output voltage in step 6.

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7.3.1.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 4, the measured output voltage SHALL less than 1V and the measured output current shall be less than 10 mA.
3. In step 6, the measured output voltage SHALL be in the range of 55.75-60V.

7.3.2 PSE operation in presence of ELC3 (off-hook phone)

This test covers the off-hook detection during normal operation, taking into account the dI/dt generated by the off-hook. Specific order in which the switches should be turned on (and turned off) is described in Section 6.1.1.7.

Test requirement: Mandatory.

7.3.2.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-4.
2. Off-hook emulator circuitry SHALL be connected with toggle switches S1…S6 in an off position.
3. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
4. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
5. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
6. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.3.2.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. Turn on switch S4.
4. Wait 1 second, then measure output voltage at the PSE (see Note 1).
5. Turn off switch S4.
6. Wait 5 seconds, then measure DC output voltage at the PSE.
7. Turn on switch S5.
8. Wait 1 second, then measure output voltage at the PSE (see Note 1).
9. Turn off switch S5.
10. Wait 5 seconds, then measure output voltage at the PSE.
11. Turn on switch S6.
12. Wait 1 second, then measure output voltage at the PSE.
13. Turn off switch S6.
14. Wait 5 seconds, then measure output voltage at the PSE.

Note 1: Due to repetitive start-up retrials of the PSE, the 1 second wait time should be increased if necessary, to avoid that the measurement coincides with the detection or classification phase of the PSE.

7.3.2.3 Report

1. The measured output voltage in steps 2, 4, 6, 8, 10, 12, 14.
2. Report whether PSE provided indication of detected ELC3 condition [yes/no].

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7.3.2.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 4, the measured output voltage SHALL be less than 1V.
3. In step 6, the measured output voltage SHALL be in the range of 55.75-60V.
4. In step 8, the measured output voltage SHALL be less than 1V.
5. In step 10, the measured output voltage SHALL be in the range of 55.75-60V.
6. In step 12, the measured output voltage SHALL be in the range of 55.75-60V.
7. In step 14, the measured output voltage SHALL be in the range of 55.75-60V.

7.3.3 PSE electrical characteristics at the PSE output

Test requirement: Mandatory.

7.3.3.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-2.
2. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
3. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
4. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
5. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.3.3.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. Using electronic load increase the current per Figure 6-7 and requirements of 6.1.1.3.
4. Measure output voltage, current and power on every step of Figure 6-7.

7.3.3.3 Report

1. The measured output voltage in step 2.
2. The measured output voltage (V_{PSE}), current (I_{PSE}) and power (P_{PSE}) in step 4.

7.3.3.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 4, the measured output voltage, current and power SHALL be according to Figure 7-1 and Figure 7-2:
    a. For $I_{PSE} \leq I_{SRimin}$, V_{PSE} SHALL be in the range of 55.75-60V.
    b. For $I_{SRimin} < I_{PSE} \leq I_{SRimax}$, PSE MAY or MAY NOT remove the V_{PSE} in the range of 55.75-60V.
    c. For $I_{PSE} > I_{SRimax}$, PSE SHALL remove V_{PSE} in the range of 55.75-60V.
    d. V_{PSE} - I_{PSE} diagram SHALL lay within the allowed tested region shown in Figure 7-1.
    e. P_{PSE} - I_{PSE} diagram SHALL lay within the allowed tested region shown in Figure 7-2.

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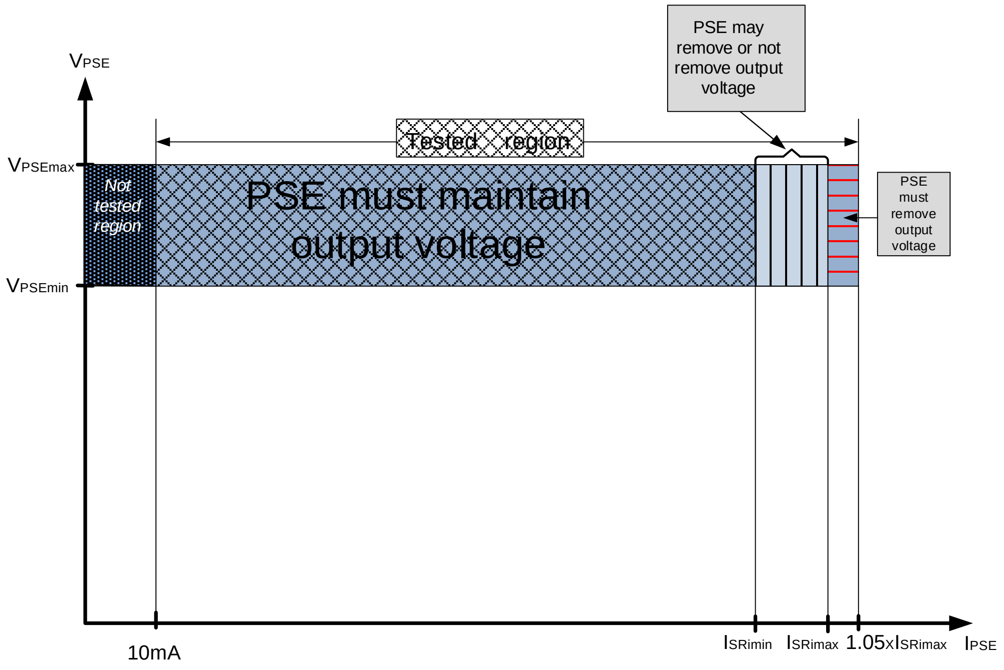

Figure 7-1 – Allowed tested region for V_{PSE}-I_{PSE} diagram

The following parameters are defined in Figure 7-1:

- V_{PSEmax} is the maximum DC voltage of PSE
- V_{PSEmin} is the minimum DC voltage of PSE
- I_{SRimax} is the maximum DC current for RPF power class SRi, i=1,2,3
- I_{SRimin} is the minimum DC current for RPF power class SRi, i=1,2,3

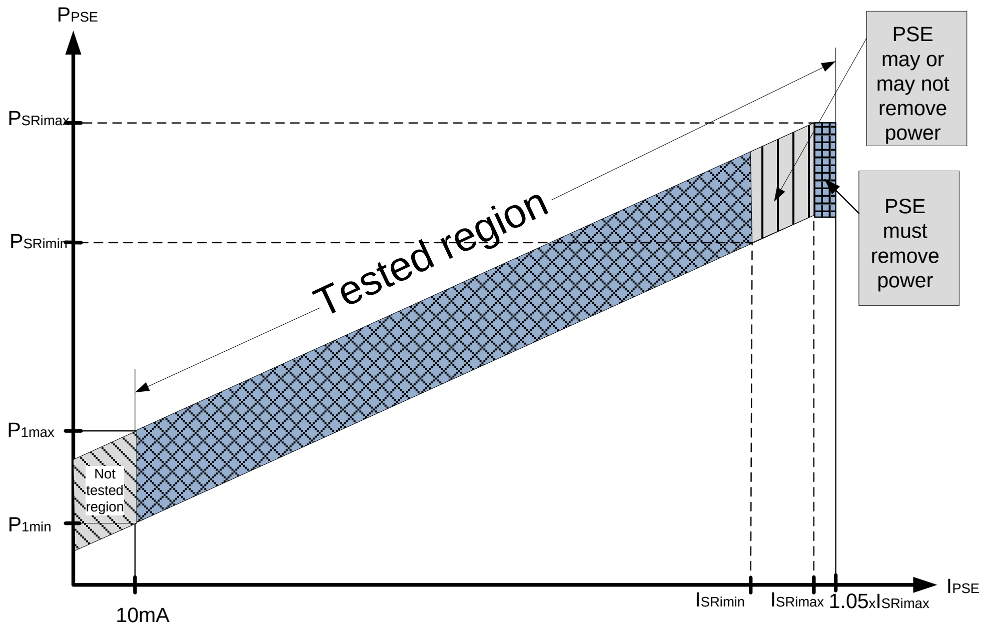

Figure 7-2 – Allowed tested region for P_{PSE}-I_{PSE} diagram

The following parameters are defined in Figure 7-2:

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- $P_{SRimax} = V_{PSEmax} \times I_{SRimax}$, i=1,2,3
- $P_{SRimin} = V_{PSEmin} \times I_{SRimin}$, i=1,2,3
- $P_{1max} = V_{PSEmax} \times 10mA$
- $P_{1min} = V_{PSEmin} \times 10mA$

Note that the gray regions in Figure 7-1 and Figure 7-2 are each indicated as “not tested” because the $I_{PSE} < I_{SRi}$=10 mA.

7.3.4 Test on PSE power class

Purpose of this test is to ensure the PSE will be in powering stage while DPU is supplying minimum power signature current equal to:

- DC current of 10mA
- Pulse current with amplitude 10mA, pulse duration 75ms and period 325ms (Table 7-1, Note 2d)

7.3.4.1 Case 1: DPU Power signature is 10mA DC current

Test requirement: Mandatory.

7.3.4.1.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-2.
2. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
3. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
4. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
5. The electronic load (I_{SRi}) SHALL be set to 10mA, see 6.1.1.3.

7.3.4.1.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. In order to set PSE current to 0mA, insert the ELC0 condition (open tip-to-ring).
4. After 5 seconds measure sensing voltage pulses and output voltage over a 5 second period.
5. Remove the ELC0 condition.
6. Wait 5 seconds, then measure output voltage at the PSE.

7.3.4.1.3 Report

1. The measured output voltage in step 2.
2. The measured sensing voltage pulses and output voltage in step 4.
3. The measured output voltage in step 6.

7.3.4.1.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 4, the measured voltage SHALL NOT exceed 30V during the 5 seconds measurement period.

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3. In step 6, the measured output voltage SHALL be in the range of 55.75-60V.

7.3.4.2 Case 2: DPU Power signature is a pulse current with amplitude 10mA, pulse duration 75ms and period 325 ms

Test requirement: Mandatory.

Test setup with DPU power signature as a pulse current is shown inFigure 6-5.

7.3.4.2.1 Test Setup

1. The PSE and DPU emulator SHALL be connected to the test setup shown in Figure 6-2.
2. The loop resistor R_{loop} SHALL be set to 43Ω +/-5%, see Table 6-7.
3. The DPU signature $R_{V\text{-}SIG}$ SHALL be set to 24.9kΩ +/-1%.
4. The RPF Power Class resistor SHALL be set to the power class that corresponds to the tested PSE power class, see Table 6-4.
5. Resistor R1 is 1100Ω +/-1% and a toggle switch S1 is ON.
6. The electronic load (I_{SRi}) SHALL be set to 0mA, see 6.1.1.3.

7.3.4.2.2 Method of Procedure

1. Apply input power to the PSE, wait until the PSE is fully operational, and connect the PSE to the test setup.
2. Wait 5 seconds, then measure output voltage at the PSE.
3. Using electronic load, set current pulses of 10mA, with load profile 75ms ON and 250ms OFF (0mA) and turn on electronic load.
4. Turn off switch S1.
5. Wait 5 seconds, then measure output voltage at the PSE.

7.3.4.2.3 Report

1. The measured output voltage in step 2.
2. The measured output voltage in step 5.

7.3.4.2.4 Expected Results

1. In step 2, the measured output voltage SHALL be in the range of 55.75-60V.
2. In step 5, the measured output voltage SHALL be in the range of 55.75-60V.

7.4 POTS Remote Copper Reconfiguration (PRP) testing

For further study.

7.5 Reverse Power Feed (RPF) Noise tests

For further study.

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Appendix II. DPU Emulator for PSE standalone testing

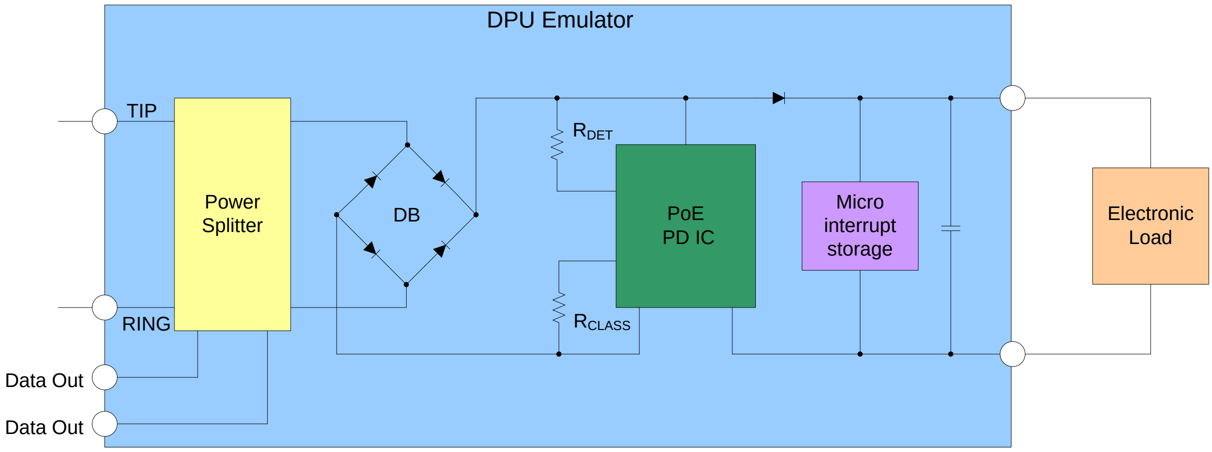

Figure 7-3 - DPU Emulator for PSE standalone testing (example)

Note:

1. Power Over Ethernet Power Device ICs commercially produced by many PoE PD IC vendors
2. R_{CLASS} resistors for e.g., PD70101 are:

Class SR1 R_{CLASS} = 133±1%

Class SR2 R_{CLASS} = 69.8±1%

Class SR3 R_{CLASS} = 45.3±1%

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